YouTube	Suite Configuration Matrix	Orcad PCB Designer Standard	Orcad PCB Designer Professional	Allegro PCB Designer
	SCHEMATIC ENTRY + DATA MANAGEMENT			
	Graphical, flat and hierarchical page editor and Picture block hierarchy	✓	✓	✓
VIDEO	OrCAD Capture Market place for Apps, Models, Symbols and more	✓	✓	✓
VIDEO	Net Groups - Complex bus definition	✓	✓	✓
VIDEO	Intelligent PDF creation	✓	✓	✓
VIDEO	AutoWire	✓	✓	✓
	44,000 Schematic symbols	✓	✓	✓
VIDEO	3D Footprint Viewer	✓	✓	✓
VIDEO	Coloured Components / nets	✓	✓	✓
	Tcl TK scripting support	✓	✓	✓
VIDEO	Online design rule check including custom DRC capability and Waive DRC	✓	✓	✓
VIDEO	Forward and back-annotation of properties / pin-and-gate swaps	✓	✓	✓
VIDEO	Schematic Part and Library editor	✓	✓	✓
VIDEO	Cross-probing and cross-placing	✓	✓	✓
VIDEO	FPGA design-in / pin import & export	✓	✓	✓
VIDEO	Multiple PCB netlist interfaces	✓	✓	✓
	SI Topology creation	✓	✓	✓
VIDEO	Digi-Key (PartLink App) Component Parametric data directly from web	✓	✓	✓
	Property editor for pins, components, nets	✓	✓	✓
VIDEO	Component Information System	CIS option	CIS option	✓
VIDEO	Windows ODBC compatible format	CIS option	CIS option	✓
	Interface to relational database and management systems	CIS option	CIS option	✓
	Centralized part number and information management system	CIS option	CIS option	✓
VIDEO	Database query for part selection and parametric properties	CIS option	CIS option	✓
VIDEO	Schematic and BOM Variants Manager (Parts not Fitted and more).	CIS option	CIS option	✓
VIDEO	ActiveParts.com over 2,000,000 schematic parts ready to place	CIS option	CIS option	✓
	CIS Database Management Interface (access control and more)	CIS Option + CIP E Option	CIS Option + CIP E Option	CIP E Option
VIDEO	Part search DIGIKEY, FARNELL, FUTURE, MOUSER, ARROW	CIS Option + CIP E Option	CIS Option + CIP E Option	CIP E Option
	PCB EDITOR	**Orcad PCB Designer Standard**	**Orcad PCB Designer Professional**	**Allegro PCB Designer**
VIDEO	Physical, Spacing, Same net, Netclass and Class to Class rules	✓	✓	✓
VIDEO	DFM Pad Entry / Exit Rules	✓	✓	✓
VIDEO	Interactive Routing using Working Layer (layer selection popup)	✓	✓	✓
VIDEO	Constraint Manager adherence feedback (Red, Green, Yellow)	✓	✓	✓
VIDEO	Multiple placement options, manual, quickplace, auto and room	✓	✓	✓
VIDEO	Placement directly from schematic, individually or window select	✓	✓	✓
VIDEO	Interactive route completion	✓	✓	✓
VIDEO	Dynamic Shapes (dynamic copper pours) Plow and Heal	✓	✓	✓
VIDEO	Snake Routing for Hex pattern ICs	✓	✓	✓
VIDEO	Push, Shove and Hug interactive editing	✓	✓	✓
VIDEO	Embedded net names	✓	✓	✓
VIDEO	Curve Routing	✓	✓	✓
VIDEO	Through Board Transparency (OpenGL)	✓	✓	✓
VIDEO	Multi-line routing (Group Routing)	✓	✓	✓
VIDEO	Fan-out generators	✓	✓	✓
VIDEO	Flip Board	✓	✓	✓
VIDEO	Dynamic pad suppression / Unused Pad removal	✓	✓	✓
VIDEO	IDF 3.0 In/Out, DXF In/Out	✓	✓	✓
VIDEO	3D viewer for selected item or complete PCB.	✓	✓	✓
VIDEO	Gerber 274X, 274D artwork Output	✓	✓	✓
VIDEO	Auto Finish (Route Completion Tool)	✓	✓	✓
	IPC2581 Import / Export	✓	✓	✓
VIDEO	Mentor® ODB++ and universal viewer	✓	✓	✓
VIDEO	DFM Checks including soldermask, solderpaste and more	✓	✓	✓
	Route cleanup, optimization (Glossing)	✓	✓	✓
VIDEO	Cross Section Editor	✓	✓	✓
	Impedance Calculator	✓	✓	✓
	Interactive / Automatic Silkscreen generation	✓	✓	✓
	Manual Design For Test (DFT) / Test Prep	✓	✓	✓
VIDEO	Component Height DRC	✓	✓	✓
VIDEO	Associative Dimensioning	✓	✓	✓
VIDEO	CAD Translators - Import PADS, PCAD, OrCAD Layout	✓	✓	✓
VIDEO	MCAD/ECAD Incremental design data exchange (IDX)	✓	✓	✓
VIDEO	Shape based curve fillet support, tapered traces		✓	✓
VIDEO	Aligment x and y for components and modules		✓	✓
VIDEO	Placement replication, template based design reuse		✓	✓
VIDEO	Differential Pairs Physical rules and routing		✓	✓
VIDEO	Constraint Regions, region based rules (Rigid-Flex; BGA regions)		✓	✓
VIDEO	Total Etch Length - Max/Min Length		✓	✓
VIDEO	Interactive Delay Tuning		✓	✓
	Automatic Design For Test (DFT) / Test Prep		✓	✓

	CAD Translators - Import Mentor® Boardstation			✓
	Max Via Count rules			✓
VIDEO	Dynamic Heads-up Display for critical rules			✓
VIDEO	Dynamic DFA rules based interactive placement			✓
VIDEO	Differential Pair Static Phase Control rules			✓
VIDEO	Offset Routing			✓
	Layer set rules			✓
	Extended (X)net rules			✓
	Estimated Crosstalk rules			✓
VIDEO	Propagation delay rules (Min/Max, Relative) for nets or groups			✓
	Pin Pair rules			✓
VIDEO	Net Scheduling, T-Point rules (pin to T-point), T-Point definition			✓
VIDEO	Via array / Shielding			✓
VIDEO	Design planning - Create hierarchical Bundles			✓
VIDEO	Design planning - Create, Edit Flows			✓
VIDEO	Design planning - Assign Flows to Layers			✓
VIDEO	Group route via pattern			✓
	Design Planning - Plan Spatial Feasibility analysis & feedback			Design Planning Option
	Design Planning - Generate Topological Plan			Design Planning Option
	Design Planning - Convert Topological plan to traces (CLINES)			Design Planning Option
	Design Planning - Plan Topological with Electrical rules			Design Planning Option
VIDEO	Auto Interactive Delay Tune (AiDT)			PCB High-Speed Option
VIDEO	Electrical Constraint rule set (ECSets) / Topology Apply			PCB High-Speed Option
VIDEO	Electrical rules (Reflection, Timing, Crosstalk)			PCB High-Speed Option
VIDEO	Package Pin Delay (for die-2-die delay) rules			PCB High-Speed Option
VIDEO	Dynamic Differential Pair Phase Control rules			PCB High-Speed Option
VIDEO	Z-Axis delay feedback			PCB High-Speed Option
VIDEO	Extended Net creation			PCB High-Speed Option
VIDEO	Advanced Constraints (formulas, relational)			PCB High-Speed Option
VIDEO	Backdrilling			PCB High-Speed Option
VIDEO	Segment over void detection			PCB High-Speed Option
VIDEO	Spread lines between voids			PCB High-Speed Option
	HDI Micro-via (spacing, stacking) rules			Miniaturization Option
	HDI micro-via inset (via-in-pad) rules			Miniaturization Option
	HDI micro-via stack editing			Miniaturization Option
	Dynamic shape based filleting, line fattening and trace filleting			Miniaturization Option
VIDEO	Hug Contour routing (Flex)			Miniaturization Option
	Single Click multiple micro- via instantiation			Miniaturization Option
	Unused micro-via removal			Miniaturization Option
	Manufacturing rule support for embedding components			Miniaturization Option
	Embedded Packaged Components			Miniaturization Option
	Support for Cavities on inner layers			Miniaturization Option
	Dual Side Contact Components			Miniaturization Option
	Vertically Placed Components			Miniaturization Option
	Removal of unassigned indirect attached vias			Miniaturization Option
	Concurrent Team Design - Layer by Layer			PCB Team Design Option
	Concurrent Team Design - Functional block partitioning			PCB Team Design Option
	Concurrent Team Design - Team design dashboard			PCB Team Design Option
	Concurrent Team Design - Soft nets			PCB Team Design Option
	Concurrent Team Design - Flexible boundaries			PCB Team Design Option
	Concurrent Team Design - Constraint Editing per Partition			PCB Team Design Option
	Swap pins on a FPGA (based on FPGA rules) in PCB Editor			FPGA System Planner
	Reoptimize pins on a FPGA (using FPGA rules)			FPGA System Planner
	Parameterized RF etch elements			PCB Analog / RF Option
	Asymmetrical Clearances			PCB Analog / RF Option
	RF Etch elements editing			PCB Analog / RF Option
	Bi-Directional interface with Agilent ADS			PCB Analog / RF Option
	ADS schematics Import Agilent into DE-HDL			PCB Analog / RF Option
	Layout-driven RF design creation			PCB Analog / RF Option
	Flexible Shape Editor			PCB Analog / RF Option
	Via Array placement on traces, shapes			PCB Analog / RF Option
VIDEO	**PSPICE SIMULATION**	**Orcad PCB Designer Standard**	**Orcad PCB Designer Professional**	**Allegro PCB Designer**
VIDEO	DC sweep, AC sweep, & transient analysis	Pspice AD	Pspice AD	Pspice AD
	Analog behavioural modelling	Pspice AD	Pspice AD	Pspice AD
	Stimulus editor	Pspice AD	Pspice AD	Pspice AD
	Model Editor for device characterization	Pspice AD	Pspice AD	Pspice AD
	Interactive waveform viewer & analyzer	Pspice AD	Pspice AD	Pspice AD
	IBIS / DML model support	Pspice AD	Pspice AD	Pspice AD
	Sensitivity: Identifies critical circuit components	Advanced Analysis	Advanced Analysis	Advanced Analysis
	Optimizer: Optimizes key circuit components	Advanced Analysis	Advanced Analysis	Advanced Analysis
VIDEO	Monte Carlo: Analyzes statistical circuit behaviour and yield	Advanced Analysis	Advanced Analysis	Advanced Analysis
	Smoke: Detects component stress	Advanced Analysis	Advanced Analysis	Advanced Analysis

	Parametric Plotter: Examine solution through nested sweeps	Advanced Analysis	Advanced Analysis	Advanced Analysis
	SIGNAL INTEGRITY	**Orcad PCB Designer Standard**	**Orcad PCB Designer Professional**	**Allegro PCB Designer**
VIDEO	Pre- & Post-route signal integrity analysis		✓	
VIDEO	Graphical topology definition and exploration		✓	
VIDEO	Interactive waveform viewer		✓	
VIDEO	Macro modelling support (DML)		✓	
VIDEO	IBIS 5.0 support		✓	
VIDEO	IBIS ICM model support		✓	
VIDEO	Spectre-to-DML		✓	
VIDEO	HSPICE-to-IBIS		✓	
VIDEO	Lossy transmission lines		✓	
VIDEO	Coupled (3 net) simulation		✓	
VIDEO	Differential pair exploration and simulation		✓	
	AUTOROUTER	**Orcad PCB Designer Standard**	**Orcad PCB Designer Professional**	**Allegro PCB Designer**
VIDEO	6 Signal Layers at a time (no board layer limit or pin limit)		✓	✓
	Shape-based or Gridded routing		✓	✓
	SMD Fanout		✓	✓
	Trace Width by Net and Net Classes		✓	✓
	45-degree / Memory Pattern Routing		✓	✓
	Interactive Routing with Shoving and Plowing		✓	✓
	Interactive Floorplanning		✓	✓
	Online Design Rule Checking		✓	✓
	Flip, Rotate, Align, Push, and Move Components		✓	✓
	Placement Density Analysis		✓	✓
	High-Speed rules based autorouting			✓
	Min/Max, matched length rules based autorouting			✓
	Pin-pair rules, Area rules based autorouting			✓
	Crosstalk controls, parallelism rules based autorouting			✓
	Differential Pair Autorouting, Automatic net shielding			✓
	High-speed rules-based autorouting			✓
	256 signal layer limit			PCB Routing Option
	DFM rules-based autorouting			PCB Routing Option
	Automatic trace spreadiing			PCB Routing Option
	ATP generation			PCB Routing Option
	Layer-specific rules-based autorouting			PCB Routing Option

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