Hours & Cost Summary

For: Robert Feranec **From:** February 15, 2011 **To:** July 15, 2011

Hours [h]		*Description*
360.93h		**TI module: HW development v1i1**
0.25		*Development board (websearch, emails)*
3.12		*TI DDR3 placement, layout, info, docs ...*
3.92	✔	*SCH: Import to Altium, setting up version control sytem, pre-compilation (cleaning errors and warnings)*
14.50	✔	*SCH: Removing peripherals, modifying current connections / connectors*
13.78	✔	*Changing: DDR3, Powers*
4.47		*Checking information about: JTAG, Ethernet,B2B connector, CPU*
36.18		*Components: Optimization, Ordering information, Footprints + Mech (height, assembly drawing)*
10.08	✔	*SCH: Updating Ethernet, comunication with Micrel, Calculations for PWR, HDMI, JTAG*
12.92	✔	*Importing SCH to PCB, Initial BOM, checking footprints*
15.70	✔	*Preliminary placement*
1.33	✔	*Checking EOL*
16.48	✔	*Preparing schematic for compilation, improving syntax, adding notes, rules, variants*
2.10		*BOM: Building BOM, Helping with Purchasing*
4.05	✔	*Updates based on feedback, checking other options, SD card option*
22.25	✔	*SCH Checking: Component pins, Pin Name Net Name, Net connection*
3.10		*PCB comunication: Stackup*
1.17		*Layout: Setting up rules*
4.37		*Mechanical: 3D model, Assembly drawing, Top and Bottom View*
34.10	✔	*Layout: DDR3 memory (connecting unconnected nets)*
50.83	✔	*Layout: Others (connecting unconnected nets)*
14.67		*Manufacturing info, Cleaning tracks, DIFF pairs length matching,*
21.62	✔	*All nets connected: Improving powers, Clearing DRC, DIFF pairs routing*
50.27	✔	*DDR3 length matching*
1.07		*Small updates, Formatting before release,*
8.97		*Finishing: Power planes, Checking manufacturability, checking gerbers*
9.63		*DDR3 Memory layout final check*

360.93 hours	**Total**